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06ES33

Third Semester B.E. Degree Examination, June/July 2011
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions selecting at least TWO from each Part.***

PART A

1 a. Staircase light is controlled by two switches, one is at the top of the stair and other at the bottom of the stairs
   i) Make a truth table for this system
   ii) Write the logic equations in the SOP form
   iii) Realize the circuit using basic gates
   iv) Realize the circuit using minimum number of NAND gates. **(08 Marks)**

   b. Simplify by using Kornaugh map and realize the circuit using basic gates
   $f(a, b, c, d) = \pi(2, 3, 4, 6, 7, 10, 11, 12)$ **(08 Marks)**

   c. Show that $ab + \overline{ac} + a\bar{b}c(ab + c) = 1$ **(04 Marks)**

2 a. Simplify using Quine Mecluskey tabulation algorithm and find out the number of prime implicants.
   $f(a, b, c, d) = \Sigma(2, 3, 4, 5, 13, 15) + d(8, 9, 10, 11)$ **(10 Marks)**

   b. Simplify using MEV technique and implicant using basic gates
   $Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}D + A\,\overline{B}\,\overline{C}\,\overline{D} + A\,\overline{B}\,\overline{C}D + \overline{A}\,\overline{B}CD + \overline{A}B\,C\,\overline{D} + ABCD + ABC\,\overline{D}$ **(10 Marks)**

3 a. With the aid of block diagram clearly distinguish between a decoder and encoder. **(05 Marks)**

   b. Design a single decode BCD adder and explain the methodology in detail. **(10 Marks)**

   c. Implement a full substractor using a decoder and two NAND gates. **(05 Marks)**

4 a. Implement $f(a, b, c, d) = \Sigma m(10, 1, 5, 6, 7, 9, 10, 15)$ using
   i) 8 : 1 MUX with a, b, c as select line
   ii) 4 : 1 MUX with a, b, as select lines **(08 Marks)**

   b. What is comparator? Design a two bit binary comparator. **(07 Marks)**

   c. Design a full adder using multiplexer
   For a full adder
   $S = \Sigma m(1, 2, 4, 7)$
   $C = \Sigma m(7, 5, 6, 7)$ **(05 Marks)**

PART B

5 a. Explain the operation of a simple S-R flip flop using NAND gates. **(10 Marks)**

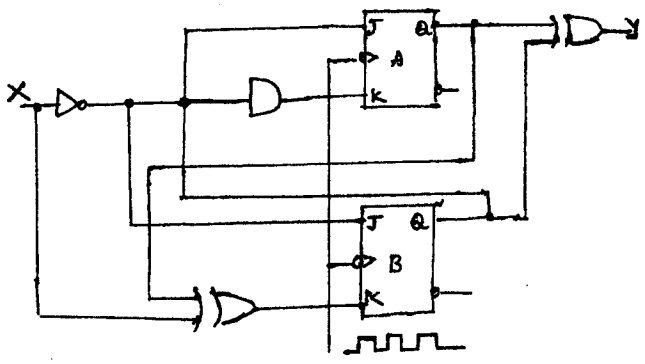
   b. What is sequential circuit? Discuss the different types of sequential circuit. **(06 Marks)**

   c. Give the logic diagram
   i) Master slave J-K flip flop
   ii) Master slave S-R flip flop **(04 Marks)**

6 a. Describe the block diagram of a mod 7 twisted ring counter and explain its operation. Give the count sequence table and the decoding logic used to identify the various states. **(10 Marks)**

   b. Design a mod-5 synchronous binary counter using clocked J-K flip flops. **(10 Marks)**

7 a. Construct the excitation table, transition table and state diagram for the Moore sequential circuit given below **(10 Marks)**



b. Compare Moore and Mealy models. **(04 Marks)**

c. Explain the Mealy model of a clocked synchronous sequential network. **(06 Marks)**

8 Write short notes on :

a. Working of switch debouncer using SR latch

b. Working of universal shift register

c. Shift registers

d. Race around condition in flip flops. **(20 Marks)**

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